PXI to ADAPT-a-SWITCH CARRIER

MODEL 1260-1XXX-Y

PUBLICATION NO. 980911

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PUBLICATION DATE: March 21, 2005

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FOR YOUR SAFETY

Before undertaking any troubleshooting, maintenance or exploratory procedure, read carefully the **WARNINGS** and **CAUTION** notices.

This equipment contains voltage hazardous to human life and safety, and is capable of inflicting personal injury.

If this instrument is to be powered from the AC line (mains) through an auto-transformer, ensure the common connector is connected to the neutral (earth pole) of the power supply.

Before operating the unit, ensure the conductor (green wire) is connected to the ground (earth) conductor of the power outlet. Do not use a two-conductor extension cord or a three-prong/two-prong adapter. This will defeat the protective feature of the third conductor in the power cord.

Maintenance and calibration procedures sometimes call for operation of the unit with power applied and protective covers removed. Read the procedures and heed warnings to avoid “live” circuit points.

Before operating this instrument:

1. Ensure the proper fuse is in place for the power source to operate.

2. Ensure all other devices connected to or in proximity to this instrument are properly grounded or connected to the protective third-wire earth ground.

If the instrument:

- fails to operate satisfactorily
- shows visible damage
- has been stored under unfavorable conditions
- has sustained stress

Do not operate until, performance is checked by qualified personnel.

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Chapter 1
SPECIFICATIONS

Introduction

Each 1260-1XXX-Y module consists of: the PXI™ to Adapt-a-Switch™ Carrier, the Mechanical Support Assembly and the specific Adapt-a-Switch Plug-in Module. The "XXX" represents the Adapt-a Switch model number while the "Y" represents the PXI bus voltage (001 = 3.3V, 002 = 5.0V).

The PXI to Adapt-a-Switch Carrier allows a single-slot Adapt-a-Switch plug-in module to be used in a PXI chassis. Two versions of the carrier exist. The –001 carrier is for a 3.3V PXI chassis while the –002 carrier is for 5V chassis. Both versions will operate in a universal chassis and conform to the PICMG 2.0 R3.0, *Compact* PCI® Specification, October 1, 1999 Including ECN 2.0-3.0-.002:Self-Describing Geography, January 23, 2002

The carrier is a small PCB assembly having 3.97" x 2" dimensions. One end of the carrier plugs into the PXI chassis backplane interfacing to the PXI bus. At the rear of the assembly is a 48-pin DIN connector that connects to the Adapt-a-Switch Plug-in Module. The carrier translates the PXI bus to the Adapt-a-Switch Plug-in interface, allowing a PXI controller to access the plug-in.

The Mechanical Support Assembly protects the Adapt-a-Switch Plug-in Module, which protrudes past the front of the PXI chassis. Since the plug-in is longer than a standard PXI module, and the carrier adds to its length, the front panel of the plug-in module protrudes approximately 5 inches past the front panel of the adjacent PXI module.

Certain PXI features are *not* supported due to the inherent design of the Adapt-a-Switch Plug-in Module. The functionality of these features resides on the J2/P2 connector of the PXI bus.

1. Reference clock (PXI_CLK10)
2. Trigger Bus (PXI_TRIG(0:7)
3. Star Trigger (PXI_STAR)
4. Local Bus (Daisy - chained, 13 lines wide)

Certain Adapt-a-Switch features are not supported due to compatibility issues with the PXI Bus.

1. Analog bus
2. Emergency Reset (1260-1120, 1260-1121A/B)
3. Adapt-a-Switch Plug-in Modules do not support SCPI when used in a PXI chassis.

Carrier Specifications

PCI Core (Carrier)	"Target Only"
System Clock	33 MHz
Data Bus	32 Bits (actual data transfers to an AaS module is byte wide on word boundaries.)
Chassis Voltage	3.3V 407933-001 5.0V 407933-002 Universal 407933-001/002
Temperature	
Operating	0°C to +50°C
Non-operating	0°C to +50°C
Relative Humidity	10 to 85%, non-condensing at < 30°C
Weight	
PXI Carrier	0.9 lbs
Mechanical Assy.	1.1 lbs.
	Dimensions
1260-1XXX Module	12.04" L x 4.436" H x .786"

Ordering Information

Listed below are part numbers that make up a generic 1260-1XXX Module. A customer who already has an Adapt-a-Switch Plug-in Module and wants to convert it to PXI use can order the PXI to AaS Carrier/Enclosure kit

ITEM	DESCRIPTION	PART #
12601XXX-001/002 Module	PXI Adapt-a-Switch Module	12601XXX-001/002
	Consists of:	
	Enclosure Assy. Kit, PXI-AaS.	407988
	PXI To AaS Carrier	407933-001/002
	Appropriate AaS Module	407XXX
Additional Manual	Manual with software drivers included	980911
PXI Carrier & Enclosure	PXI to AaS Carrier/Enclosure Kit	408000-001/002
	Consists of:	
	Enclosure Assy. Kit, PXI-AaS.	407988
	PXI To AaS Carrier	407933-001/002

Applicable Documents

1.) PICMG 2.0 R3.0, *Compact*PCI® Specification, October 1, 1999 Including ECN 2.0-3.0-.002:Self-Describing Geography, January 23, 2002

2.) PXI™ Hardware Specification, Rev 2.2 Sept 22, 2004

3.) PXI™ Software Specification, Rev 2.1 Feb. 4, 2003

4.) PXI™ Module Description File Specification, PXI-4, Rev. 1.0, Spet 25, 2003

5.) VISA for PXI Specification, PXI-3, Sept. 25, 2003

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Chapter 2

INSTALLATION INSTRUCTIONS

Unpacking and Inspection

1. Remove the 1260-1XXX module and inspect it for damage. If any damage is apparent, inform the carrier immediately. Retain shipping carton and packing material for the carrier's inspection.

2. Verify that the pieces in the package you received contain the correct 1260-1XXX module option and the 1260-1XXX Users Manual. Notify Racal Instruments if the module appears damaged in any way. Do not attempt to install a damaged module into a PXI chassis.

3. The 1260-1XXX module is shipped in an anti-static bag to prevent electrostatic damage to the module. Do not remove the module from the anti-static bag unless it is in a static-controlled area.

Reshipment Instructions

1 Use the original packing material when returning the 1260-1XXX module to Racal Instruments for servicing. The original shipping carton and the instrument's packing material will provide the necessary support for safe reshipment.

2 If the original packing material is unavailable, wrap the 1260-1XXX Module in an ESD Shielding bag.

3 Reship in either the original or a new shipping carton.

Module Installation

Insure that the two nylon brackets used to secure the 48-pin DIN mating connectors on the carrier and Adapt-a-Switch Plug-in Module are in place. Each bracket requires two bolts to be inserted into the existing holes in the connectors. The brackets prevent the two modules from coming apart during insertion and removal.

The Support Assembly protects the Adapt-a-Switch Plug-in Module, which protrudes past the front of the PXI chassis. The assembly is fastened to the faceplate of the Adapt-a-Switch Plug-in Module using two screws. **Figure 2-1** depicts the mechanical assembly of the carrier, Support Assembly and Adapt-a-Switch Plug-in Module.

After the carrier and Support Assembly are determined to be secure, the plug-in module may insert into the PXI chassis. The carrier will fit properly between the chassis card guides. The Adapt-a-Switch module is narrower than the chassis card guides and is aligned to fit only into the top card guide of the chassis. When inserting the module into the chassis take care that the module is not skewed. Two screws secure the Support Assembly (and the Plug-in Module) to the PXI chassis. **Figure 2-2** depicts the mechanical assembly of the carrier, Support Assembly and Adapt-a-Switch Plug-in Module when installed in the PXI chassis.

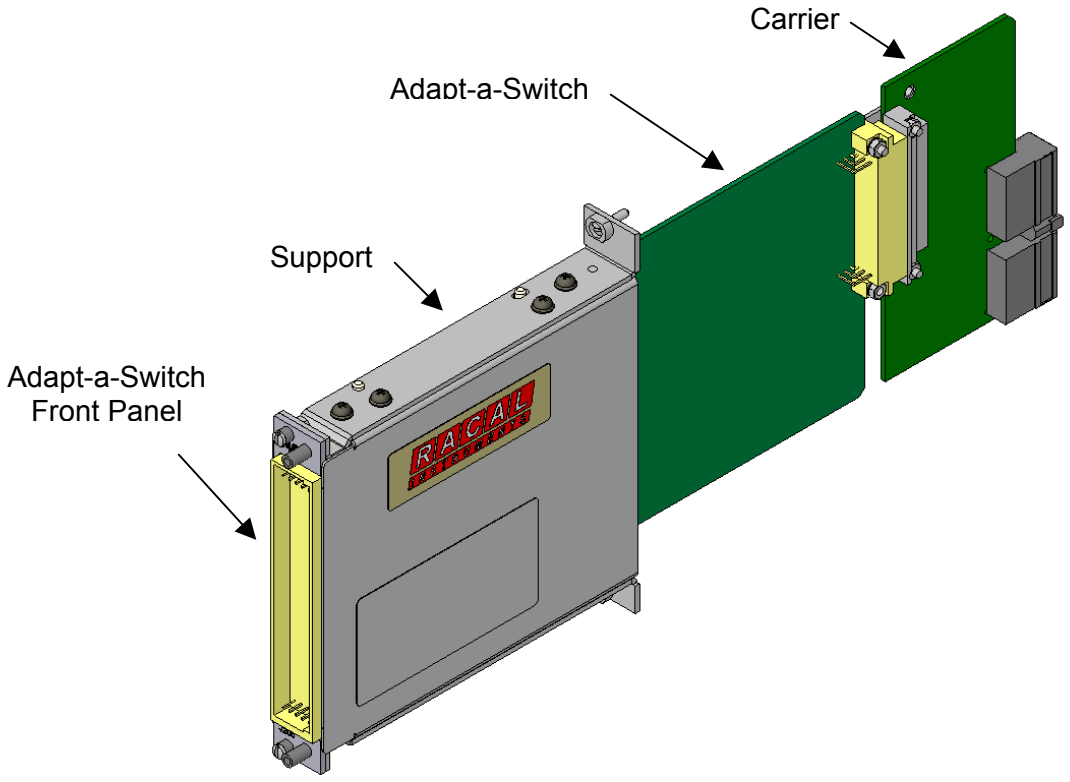


Figure 2-1 Carrier with Adapt-a-Switch Plug-in

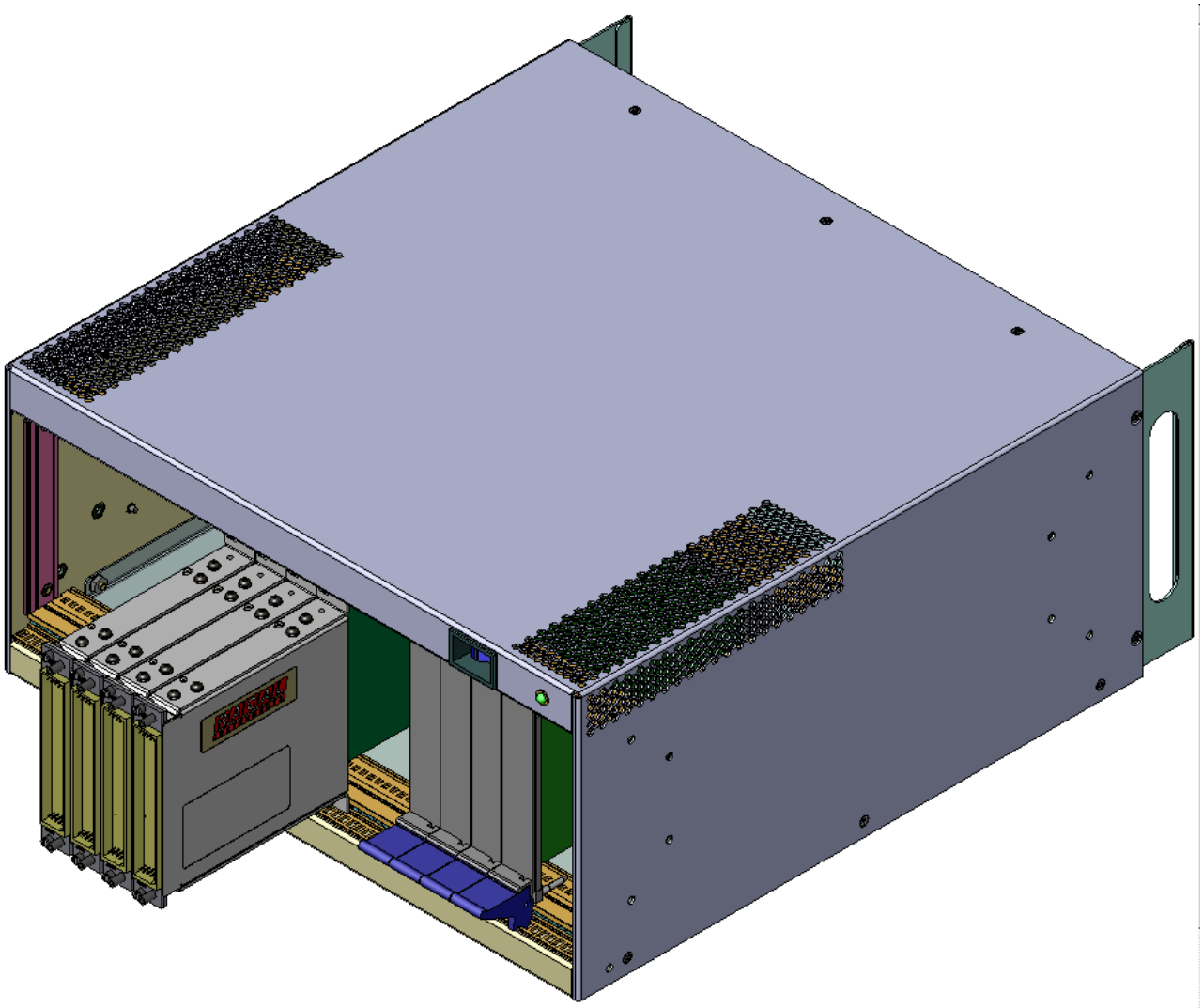


Figure 2-2 Carrier and Adapt-a-Switch Plug-in Module in a PXI Chassis

PXI to Adapt-a-Switch Carrier / Enclosure Kit

A customer who already has an Adapt-a-Switch Plug-in Module and wants to convert it to PXI use can order the PXI to AaS Carrier/Enclosure kit (408000-001/002). The kit includes everything minus the Adapt-a-Switch Plug-in Module.

Figure 2-3 is the assembly drawing of the carrier/enclosure kit. The Mechanical Support Assembly comes pre-assembled. Mounting the Mechanical Support Assembly to the faceplate of the Adapt-a-Switch Plug-in Module and securing the supplied nylon brackets to the 48-pin DIN connector is the only assembly required.

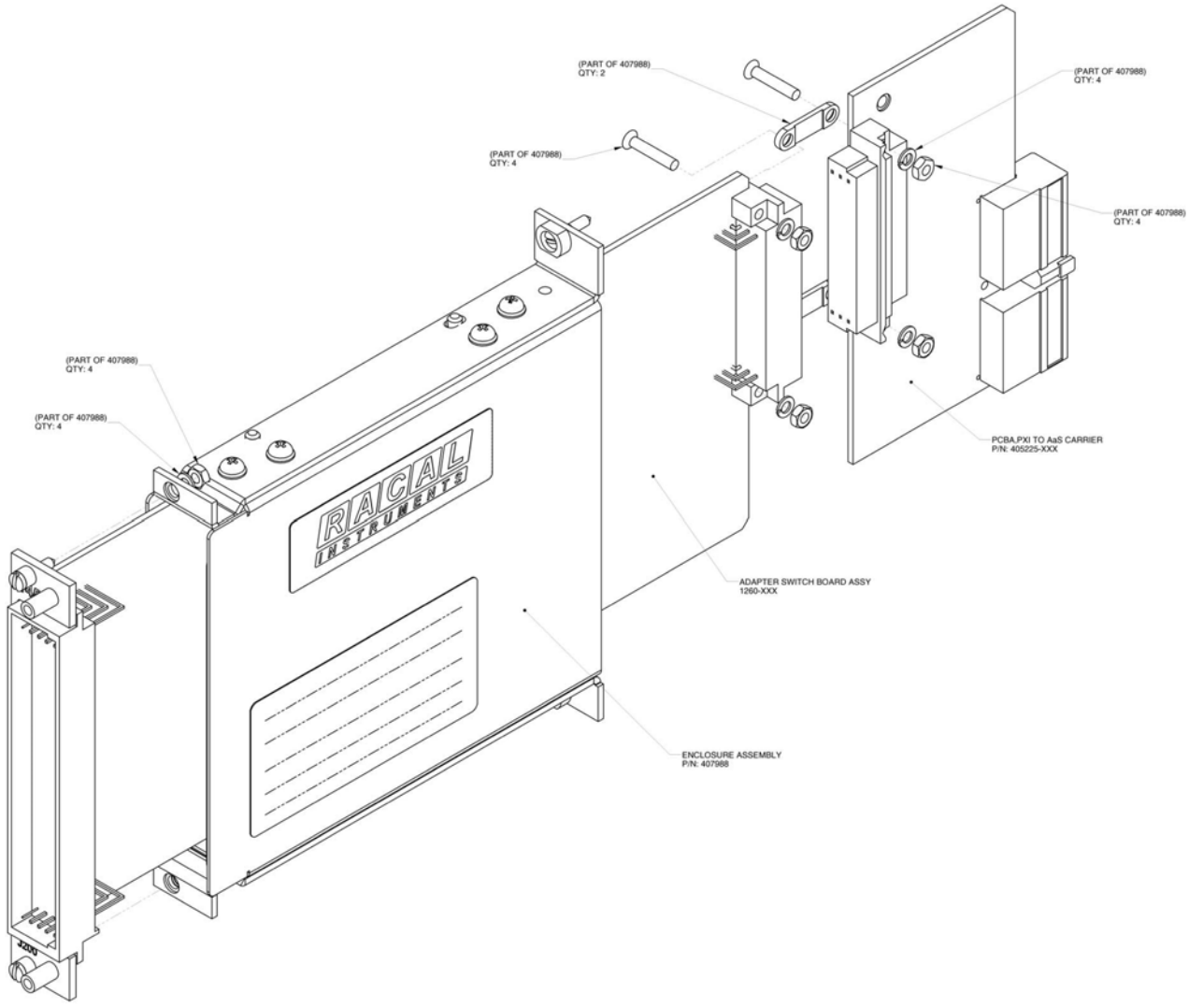


Figure 2-3 PXI Carrier/Enclosure Kit Assembly Drawing

Chapter 3
MODULE OPERATION

Operating Mode

The PXI to Adapt-a-Switch Carrier allows a single-slot Adapt-a-Switch Plug-in Module to be used in a PXI chassis. The carrier translates the PXI bus to an Adapt-a-Switch interface and allows a PXI system to communicate with the Adapt-a-Switch Plug-in Module.

When communicating with an Adapt-a-Switch Plug-in Module, only *register-based* mode is supported. In the *register-based* mode, the user writes directly to the control registers on the Adapt-a-Switch Plug-in Module. This is accomplished by setting the BAR0 register, located in the PXI carrier's configuration area, to the memory address where the Adapt-a-Switch Module will reside. This base address is then used for addressing the registers and descriptor file in the Adapt-a-Switch Module.

For specific information regarding the programming of an Adapt-a-Switch Plug-in Module, refer to the programming section in the manual for that particular Adapt-a-Switch Plug-in Module.

PCI Configuration Access

Each functional PCI device implements a set of up to two hundred and fifty-six 8-bit registers that are used during system initialization to configure the PCI device for proper operation in the system. To access a PCI device's configuration registers, a PCI configuration read or write command must be initiated on the PCI bus and the device must sense its IDSEL input asserted during the address phase. IDSEL acts as a chip-select and the contents of the AD bus are used to select the PCI device and the corresponding device's configuration register.

There are two types of configuration accesses that can be implemented in a PCI system. The type 'zero' access is used to configure a device on the PCI bus the configuration access is run on. The type 'one' access is used to configure a device on a lower-level PCI bus in a system with hierarchical PCI buses. The 1260-1XXX implements type 'zero' configuration accesses only.

Type Zero Configuration Access

The type 'zero' configuration access is used to configure a PCI device on the same PCI bus that the access is being run. When the PCI bridge initiates a configuration access on the PCI bus, it places the configuration address information on the AD bus and the configuration command on the C/BE#[3:0] bus. For a configuration read cycle, the contents of the C/BE#[3:0] bus is "1010"b. For a configuration write cycle, the C/BE#[3:0] bus is set to "1011"b. **Figure 3-1** illustrates the contents of the AD bus during the address phase of a type 'zero' configuration access.

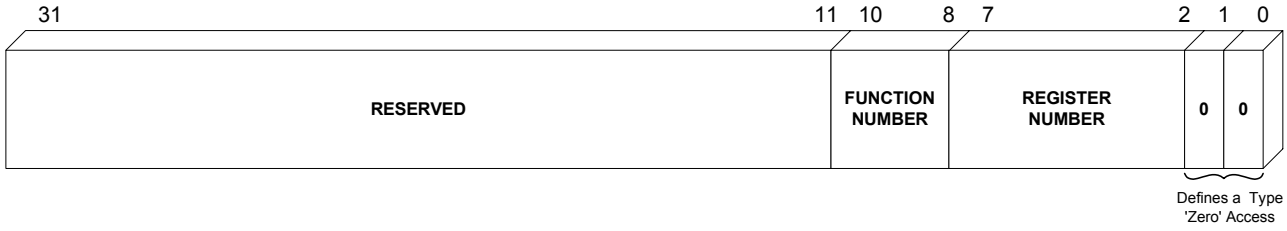


Figure 3-1 Contents of the AD Bus During Address Phase of a Type Zero Configuration Access

In order to be selected as the target of a configuration access, a PCI device must sample its device-specific IDSEL input asserted by the bridge during the address phase. It must also be a type ‘zero’ configuration access as specified by AD[1:0] being both zero. If its IDSEL is not asserted or AD[1:0] is not “00”b, the device will ignore the access.

If both the above conditions are met, address bits AD[10:8] are used to select one of eight functions within a multi-function physical device. The 1260-1XXX is a single function device so AD[10:8] must be set to “000”b. Address bits AD[7:2] are used to select one of sixty-four configuration double-word addresses within the target function. The command on the C/BE#[3:0] bus during the address phase identifies it as a configuration read or write. During the data phase, the four byte enables, C/BE#[3:0], are used to select the exact configuration registers within the currently addressed configuration double-word. The data to be transferred between the bridge and the target configuration locations is transferred during the data phase.

Configuration Register Definition

Each functional PCI device possesses a block of two hundred fifty-six configuration addresses reserved for implementation of its configuration registers. The format of the first sixty-four locations is predefined by the PCI specification. This area is referred to as the device’s configuration header region. **Figure 3-2** illustrates the format of a functional device’s header region. The registers within this range are used to identify the device, control its PCI functions and sense its PCI status in a generic manner. The remaining one hundred and ninety-two locations are device specific.

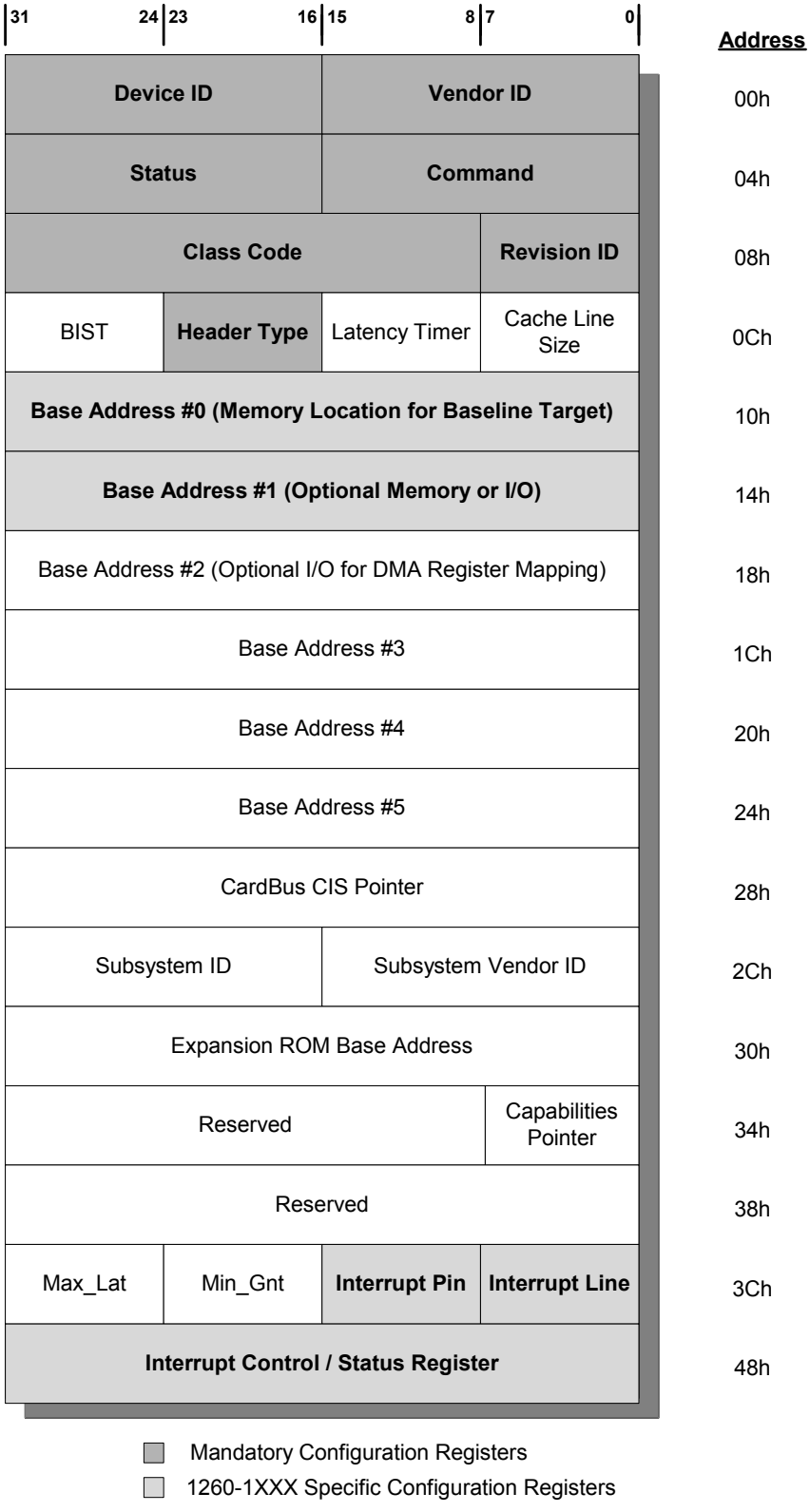


Figure 3-2 PCI Configuration Header

Mandatory Header Registers

The following sections describe the mandatory configuration registers that must be implemented in every PCI device.

Vendor ID Register (00h)

This 16 bit read-only register identifies the manufacture of the device. The vendor ID number is assigned by a central authority, which controls issuance of numbers. The value assigned to Racal Instruments is "190C"h and is hard-wired inside the FPGA core.

Device ID Register (02h)

This 16 bit read-only register identifies the device type as assigned by the manufacture. The value assigned to 1260-1XXX is "01AE"h.

Command Register (04h)

This register provides basic control over the device's ability to respond to PCI accesses. Only bits 10:0 are currently defined in this 16-bit register. Bits 15:11 are reserved for future use. After reset, all bits in this register are typically set to zero. This effectively disables the device until it is configured and enabled by the configuration software. Not all bits in this register are read/write capable. Certain bits are read-only. **Figure 3-3** and **Table 3-1** describe these bits and how they should be set by the configuration software for operation of the 1260-1XXX.

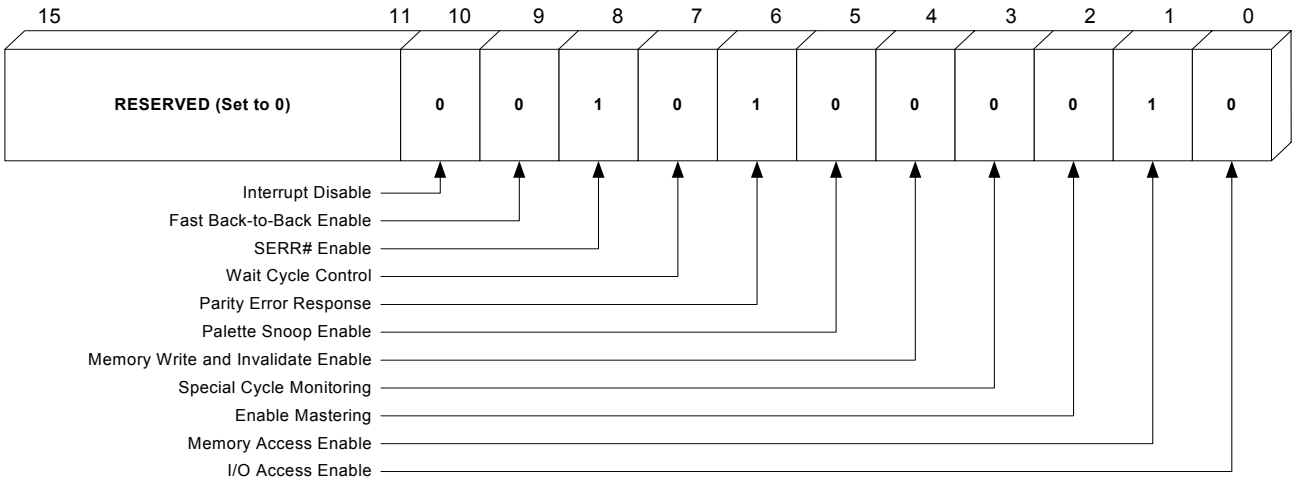


Figure 3-3 Command Register Bit Assignment for the 1260-1XXX

Bit	Type	Function
0	RW	I/O Space A value of '0' disables the device's response to I/O space addresses. Set to '0' after reset. For the 1260-1XXX, this bit should be set to '0'.
1	RW	Memory Space A value of '0' disables the device's response to memory space addresses. Set to '0' after reset. For the 1260-1XXX, the configuration software should set this bit to '1'.
2	RW (RO)	Bus Master When set to '1' enables the PCI device to act as a bus master. For a Target–only device like the 1260-1XXX, this bit is read-only and is set to '0'.
3	RO	Special Cycles The 1260-1XXX does not support special cycles. This bit is set to '0'.
4	RO	Memory Write and Invalidate Enable The 1260-1XXX does not support Memory Write and Invalidate. This bit is set to '0'.
5	RO	VGA Palette Snoop The 1260-1XXX does not support a VGA peripheral. This bit is set to '0'.
6	RW	Parity Error Response When '0' the device ignores parity errors. When set to '1' normal parity checking is performed. Set to '0' after reset. For the 1260-1XXX, the configuration software should set this bit to '1'.
7	RO	Wait Cycle Control The 1260-1XXX does not support data-stepping. This bit is set to '0'.
8	RW	SERR# Enable When '0' the SERR# driver is disabled. Set to '0' after reset. For the 1260-1XXX, the configuration software should set this bit to '1'.
9	RO	Fast Back-to-Back Enable The 1260-1XXX does not support Fast Back-to-Back transactions. This bit is set to '0'.
10	RW	Interrupt Disable When '1' prevents the device from asserting INTA# output. Set to '0' after reset. For the 1260-1XXX, the configuration software should set this bit to '0'.
15-11	RO	Reserved Set to all '0's.

Note: RW = Read and Write, RO = Read Only

Table 3-1 Command Register Bit Definitions

Status Register (06h)

This register tracks the status of PCI bus-related events. A device must only implement the bits that relate to its functionality. Not all bits in this register are read-write capable. Certain bits are read-only. Writes to this register are handled differently from the norm. The read/write bits in this register can be cleared by witting a '1' to appropriate the bit. **Figure 3-4** and **Table 3-2** describe these bits.

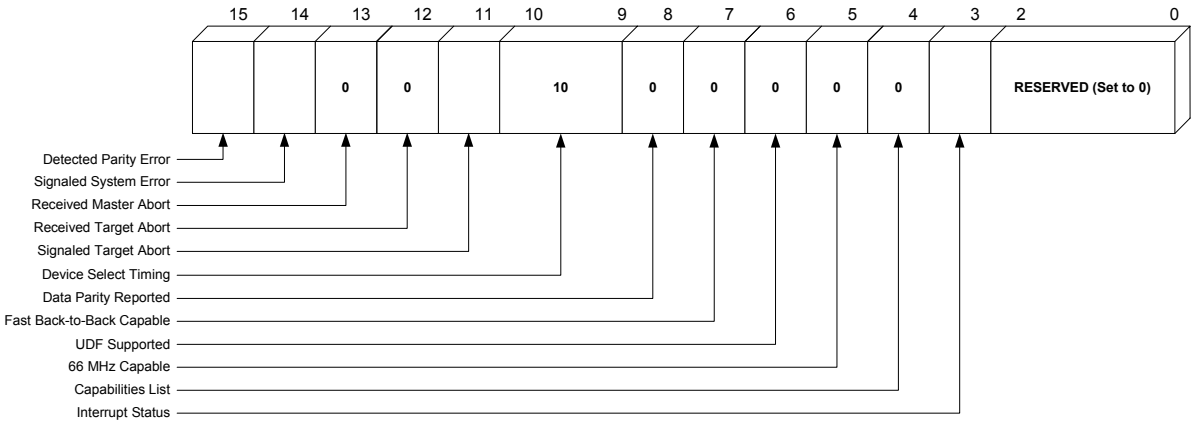


Figure 3-4 Status Register Bit Assignment for the 1260-1XXX

Bit	Type	Function
2-0	RO	Reserved Set to all '0's.
3	RO	Interrupt Status This bit reflects the status of the INTA# output.
4	RO	Capabilities List The 1260-1XXX does not support Capabilities List. This bit is set to '0'.
5	RO	66 MHz Capable Currently the 1260-1XXX does not support a 66 MHz clock rate. This bit is set to '0'.
6	RO	UDF Supported The 1260-1XXX does not support User Definable Features. This bit is set to '0.
7	RO	Fast Back-to-Back Capable The 1260-1XXX does not support Fast Back-to-Back transactions. This bit is set to '0'.
8	RO	Data Parity Error Detected For a Target-only device like the 1260-1XXX, this bit is read-only and set to '0'.
10-9	RO	DEVSEL# Timing Set to '10' for slow device response.
11	RW	Signaled Target Abort Set to '0' at system reset. This bit is set to a '1' whenever a 1260-1XXX cycle is aborted.
12	RO	Received Target Abort For a Target-only device (1260-1XXX) this bit is read-only and set to '0'.
13	RO	Received Master Abort For a Target-only device like the 1260-1XXX, this bit is read-only and set to '0'.
14	RW	Signaled System Error Set to '0' at system reset. This bit is set '1' whenever the SERR# signal is asserted by the 1260-100X.
15	RW	Detected Parity Error Set to '0' at system reset. This bit is set '1' whenever a parity error, address or data is detected by the 1260-1XXX, regardless of the value of bit 6 in the Command Register.

Note: RW = Read and Write, RO = Read Only

Table 3-2 Status Register Bit Definitions

Revision ID Register (08h)

This read-only register contains an 8-bit value that defines the revision number of the 1260-1XXX. Initially this value is set to "01"h. If a revision change has been made to either the 1260-1XXX PCB or FPGA, this value will be incremented.

Class Code Register (09h)

This 24-bit read-only register is divided into three 8-bit registers: base class, sub-class and programming interface. It identifies the basic function of the device (e.g., a mass storage controller), a more specific device classification (e.g., IDE controller), and in some cases, a register-specific programming interface (such as the VGA register set.) The upper byte defines the basic class type, the middle byte defines a sub-class within the basic class and the lower byte defines the programming interface. The defined values for the basic class code register are listed in **Table 3-3**.

Class	Description
00h	Devices built before class codes were defined (before Revision 2.0 of the spec.)
01h	Mass storage controller
02h	Network controller
03h	Display controller
04h	Multimedia device
05h	Memory controller
06h	Bridge device
07h-FEh	Reserved
FFh	Device does not fit any of the defined classed codes.

Table 3-3 Defined Class Codes

The 1260-1XXX does not fit into any of the basic class type. A read from the Class Code Register back the following values for the 8-bit registers:

Base Class Register - "FF"h

Sub-Class Register - "00"h

Programming Interface Register - "00"h

Header Type Register (0Eh)

This 8-bit read-only register defines the format of bytes 10h through 3Fh of the device's configuration header. In addition, bit seven defines the device as a single function (bit seven = 0) or multi-function (bit seven = 1) device. Currently the only format defined is a header type "00"h as pictured in **Figure 3-2**. Since the 1260-1XXX is a single function device, a read from this location will give back a value of "00"h.

Optional Header Registers

The following sections describe optional configuration registers. The 1260-1XXX implements only the registers which affect its functionality.

Memory Base Address Register (10h) Base Address #0

Base Address Register #0 defines the memory address space that the Adapt-a-Switch Plug-in Module resides. It is through this address space that a PXI system is able to communicate with the registers in the plug-in module.

In this read/write register, bit zero defines the base address register as memory (bit set to '0'). Bits 2:1 define where the block of memory can be located: in the first MByte of memory, anywhere in the 32-bit memory space, or anywhere in the 64-bit memory space. Bit three defines the block of memory as prefetchable or not. Bits 31:4 are used to determine the size of the memory block and to set the starting address. **Figure 3-5** and **Table 3-4** describe these bits.

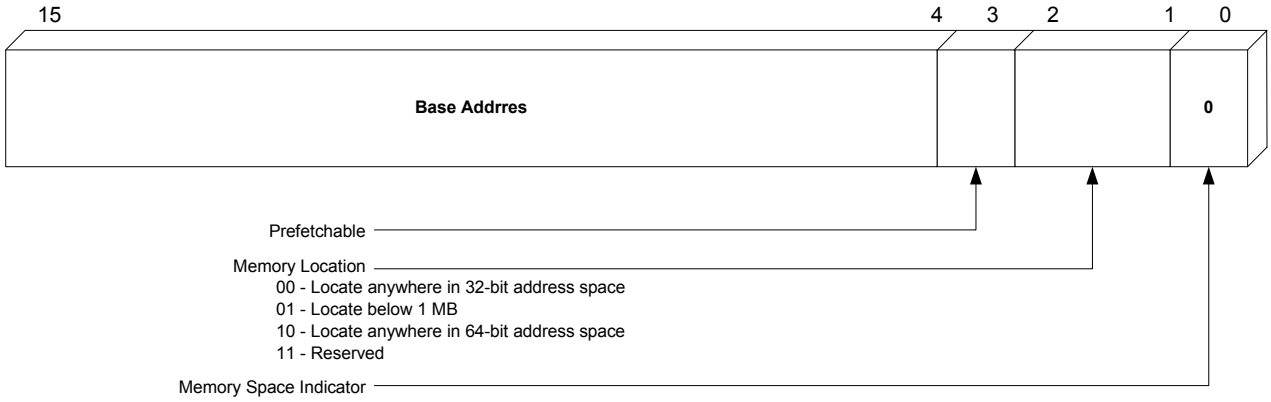


Figure 3-5 Memory Base Address Register Bit Assignments

Bit	Type	Function
0	RO	Set to '0' to indicate this is a memory base register.
2-1	RO	Set to '00' to indicate mapping into any 32-bit address space.
3	RO	Set to '0' to indicate the 1260-1XXX does not allow prefetching on read transactions.
9-4	RO	Set to all zeros indicating the 1260-1XXX uses a 1 KB memory block size.
31-10	RW	Programmable location for the 1 KB address space. To determine a hit to the 1260-1XXX, these bits are compared to PCI address bits 31-10.

Table 3-4 Memory Base Address Register Bit Definitions

Memory Block Size and Assigning Address Range (Plug-in Module)

The 1260-1XXX uses memory mapped I/O to transfer data to and from an Adapt-a-Switch module. In order for this to happen, Base Register #0 (10h) must be set up as a memory base register (bit zero is set to '0'.) The size and type of the address space required can be determined by writing all ones to a base address register then reading from the register. By scanning the returned value of the base register, starting at bit 4 upwards, the programmer can determine the size of the required address space. The binary weighted value of the first bit that is set to '1' indicates the amount of space.

As an example, assume that "FFFFFFFF"h is written to the 1260-1XXX's base address register #0, at configuration address 10h. For the PXI to AaS Carrier, the value read back is "FFFFFC00"h. Bit zero is a '0' so the device requires memory address space. Bits 2:1 are "00"b, indicating that the memory can be located anywhere within the 32 bit address space (4 GB). Bit three is set to '0' so the memory doesn't support prefetching. Scanning upwards, starting at bit four, bit ten is the first bit set to '1'. The binary weighted value of this bit is 1,024, indicating that the device requires 1 KB of memory space.

After determining the size and type of address space that the device requires, the programmer can specify the starting address by writing the appropriate value for bits 31:10 to the register. Bits 31:10 are then used by the device in comparing addresses during memory transactions on the PCI bus.

Memory Base Address Register (14h) Base Address #1

Base Address Register #1 defines the memory address space that a general-purpose timer resides. This timer is internal to the PXI to AaS Carrier and can be used for determining relay-settling time.

In this read/write register, bit zero defines the base address register as memory (bit set to '0'). Bits 2:1 define where the block of memory can be located: in the first MByte of memory, anywhere in the 32-bit memory space, or anywhere in the 64-bit memory space. Bit three defines the block of memory as prefetchable or not. Bits 31:4 are used to determine the size of the memory block and to set its starting address. **Figure 3-5** and **Table 3-4** describe these bits.

Memory Block Size and Assigning Address Range (Timer)

The PXI to AaS Carrier uses memory mapped I/O to transfer data to and from the general-purpose timer. In order for this to happen, Base Register #1 (14h) must be set up as a memory base register (bit zero is set to '0'.) The size and type of the address space required is determined in the same manner as Base Address Register #0. The address space for the timer is set to 256 bytes by the carrier.

Writing a "FFFFFFFF"h to Base Address Register #1, at configuration address 14h will give a value read back as "FFFFFF00"h. Bit zero is a '0' so the device requires memory address space. Bits 2:1 are "00"b, indicating that the memory can be located anywhere within the 32 bit address space (4 GB). Bit three is set to '0' so the memory doesn't support prefetching. Scanning upwards, starting at bit four, bit eight is the first bit set to '1'. The binary weighted value of this bit is 256, indicating that the device requires 256 bytes of memory space.

After determining the size and type of address space that the device requires, the programmer can specify the starting address by writing the appropriate value for bits 31:8 to the register. Bits 31:8 are then used by the device in comparing addresses during memory transactions on the PCI bus.

Interrupt Line Register (3Ch)

This 8-bit read/write interrupt line register is used to identify which of the interrupt request lines on the system interrupt controller the 1260-1XXX's PCI interrupt request line (as specified in its Interrupt Pin Register) is connected to. In a PCI environment, for example, the values zero (00h) through fifteen (0Fh) in this register correspond to IRQ0 through IRQ15.

The operating system or device driver can examine the 1260-1XXX's interrupt pin and interrupt line registers to determine which system interrupt request line the 1260-1XXX will use to issue requests for service.

Interrupt Pin Register (3Dh)

This 8-bit read-only register defines which of the four PCI interrupt request lines, INTA# through INTD#, the 1260-1XXX is connected to. The values one through four correspond to PCI interrupt request lines INTA# through INTD#. In the case of the 1260-1XXX, a value of 01h will be returned indicating that the 1260-1XXX is connected to the PCI interrupt request line INTA#.

Interrupt Control/Status Register (48h)

This 32-bit read/write register is used to enable and give status on the PCI interrupt request line INTA#. Of the 32-bits, only bits 9 and 8 are used. When an Adapt-a-Switch Plug-in Module or the general-purpose timer generates an interrupt request, the signal is fed to the 1260-1XXX FPGA's internal EXT_INT# signal. Bit 8 of this register shows the status of the EXT_INT# signal. If the bit 8 is set, the EXT_INT# is asserted. An INTA# interrupt will be generated if bit-9 of this register is set when the EXT_INT# signal goes true. When resetting an interrupt request, software should both the Adapt-a-Switch or the timer IRQ and bit-8 of this register. **Figure 3-6** and **Table 3-5** describe these bits.

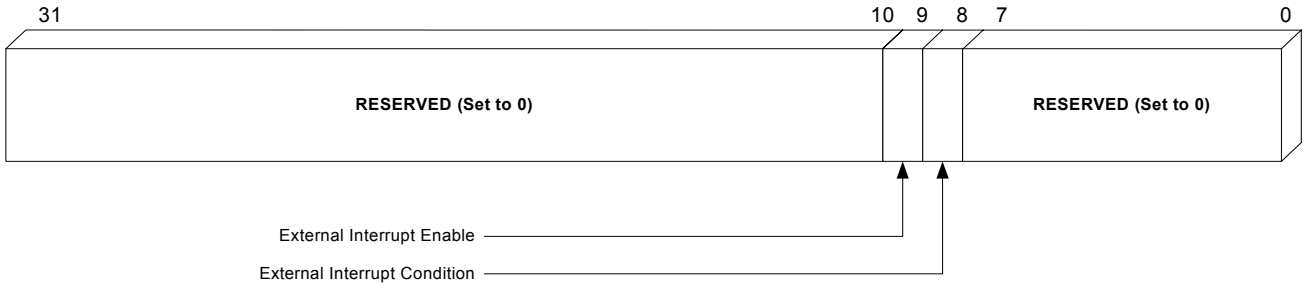


Figure 3-6 Interrupt Control/Status Register Bit Assignments

Bit	Type	Function
7-0	RO	Reserved Set to all '0's.
8	RW	External Interrupt Condition A '1' in this bit indicates an active external interrupt condition (assertion of EXT_INT#). The bit can be cleared by writing a '1' to this bit position. This bit is set to '0' after a system reset.
9	RW	External Interrupt Enable Writing a '1' to this bit enables support for the external interrupt signal. Writing a '0' to this bit disables external interrupt support. This bit is set to '0' after a system reset.
31-10	RO	Reserved Set to all '0's.

Table 3-5 Interrupt Control/Status Register Bit Definitions

Chapter 4
BUS TRANSACTIONS

Data Transfers

The 1260-1XXX allows data transfers to take place between a PXI host system and an Adapt-a-Switch Plug-in Module. For this to take place, the 1260-1XXX must perform both a bus-conversion along with data steering. PCI transfers data on a bus that is 32-bits wide (doubleword.) An Adapt-a-Switch module transfers data one byte at a time and is transferred on word boundaries (even byte boundaries.) For a data transfer to work properly, software must insure that data will be transferred one byte at a time on the PCI bus. In addition, the software must have the byte on a word boundary. **Figure 4-1** shows the location of the byte to be transferred within a 32-bit PCI data transfer for both an even and odd word boundaries.

The PCI uses addressing based on doubleword transfers. Address bits AD1 and AD0 are don't cares and are set to '0'. The Adapt-a-Switch bus uses addressing based on word transfers. This means that bit HA0 of the Adapt-a-Switch bus is a don't care and is set to '0'. However, HA1 is part of the address on the Adapt-a-Switch bus. Address bit HA1 needs to be generated from information on PCI bus and passed along to the Adapt-a-Switch bus. This is accomplished by using the states of C/BE2# and C/BE0# to determine the value of HA1. The following scenario illustrates the address transition from the PCI bus to the Adapt-a-Switch bus:

AD[31:10] are used by the 1260-1XXX's comparator to determine a hit.

AD[9:2] of the PCI bus => HA[9:2] of the Adapt-a-Switch bus

If C/BE0# is asserted, '0' => HA1 of the Adapt-a-Switch bus

If C/BE2# is asserted, '1' => HA1 of the Adapt-a-Switch bus

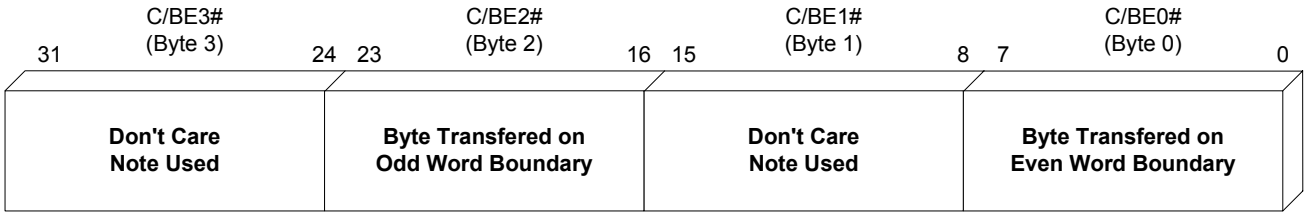


Figure 4-1 Word Boundary Byte Transfers on the PCI Bus

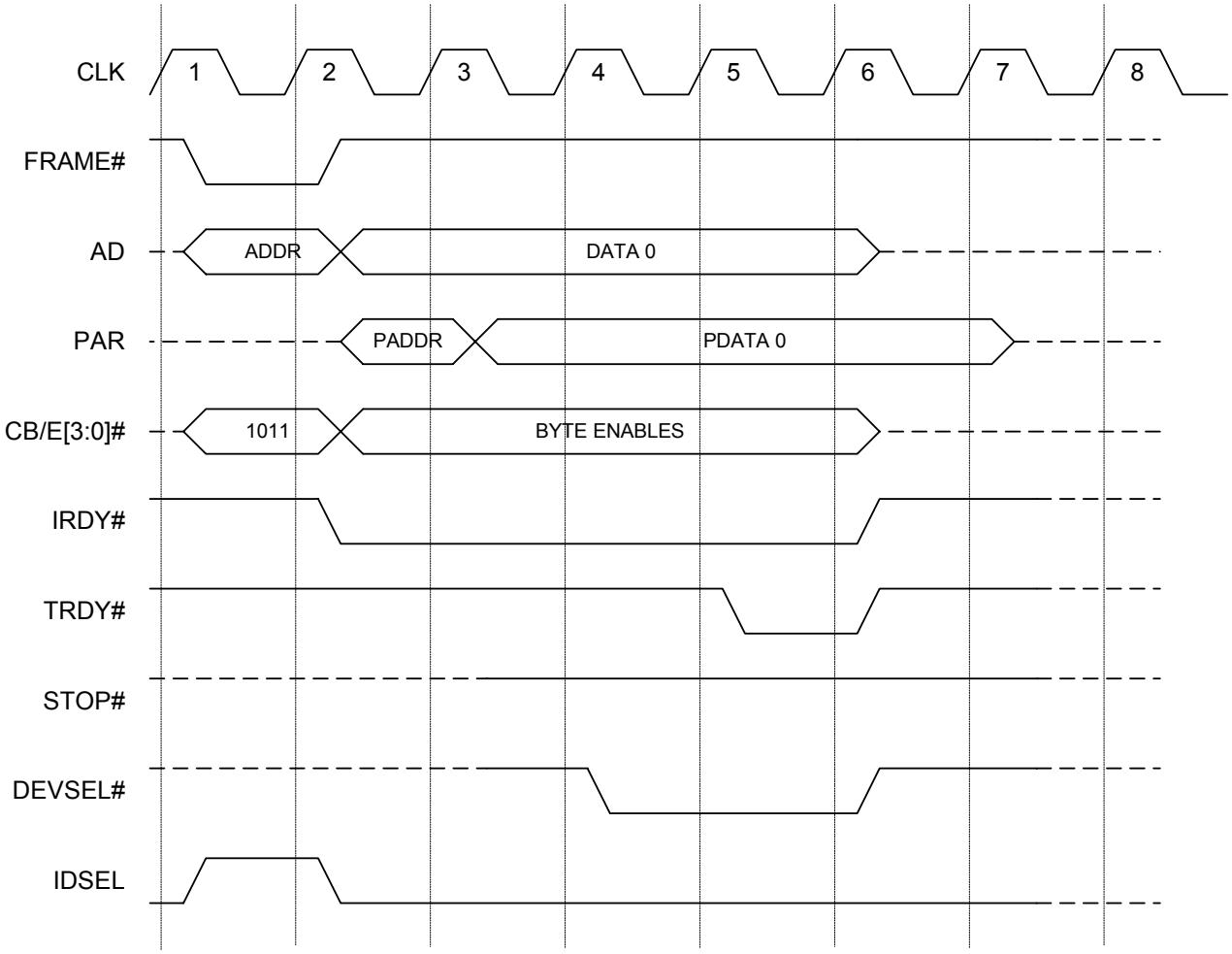
PXI (PCI) Bus

The PCI bus was founded on the premise of providing high-speed data transfers. All PCI data transfers are block data oriented and is accomplished using burst transfers. By nature, an Adapt-a-Switch module is not capable of burst transfers. Instead, the Adapt-a-Switch module transfers data on a byte-by-byte basis. The 1260-1XXX handles this situation by controlling the PCI data transfers to a burst of one (single transfer.) In addition, software must assure that only a single byte of data is transferred during the data phase of a 32-bit doubleword.

The 1260-1XXX supports two types of PCI bus transfers. These transfers consist of configuration cycles and memory cycles. Since I/O space is limited in the PC environment, memory mapped I/O (memory cycles) are used in passing data to the Adapt-a-Switch module. The following sections cover each type of PCI bus cycle.

Configuration Cycles

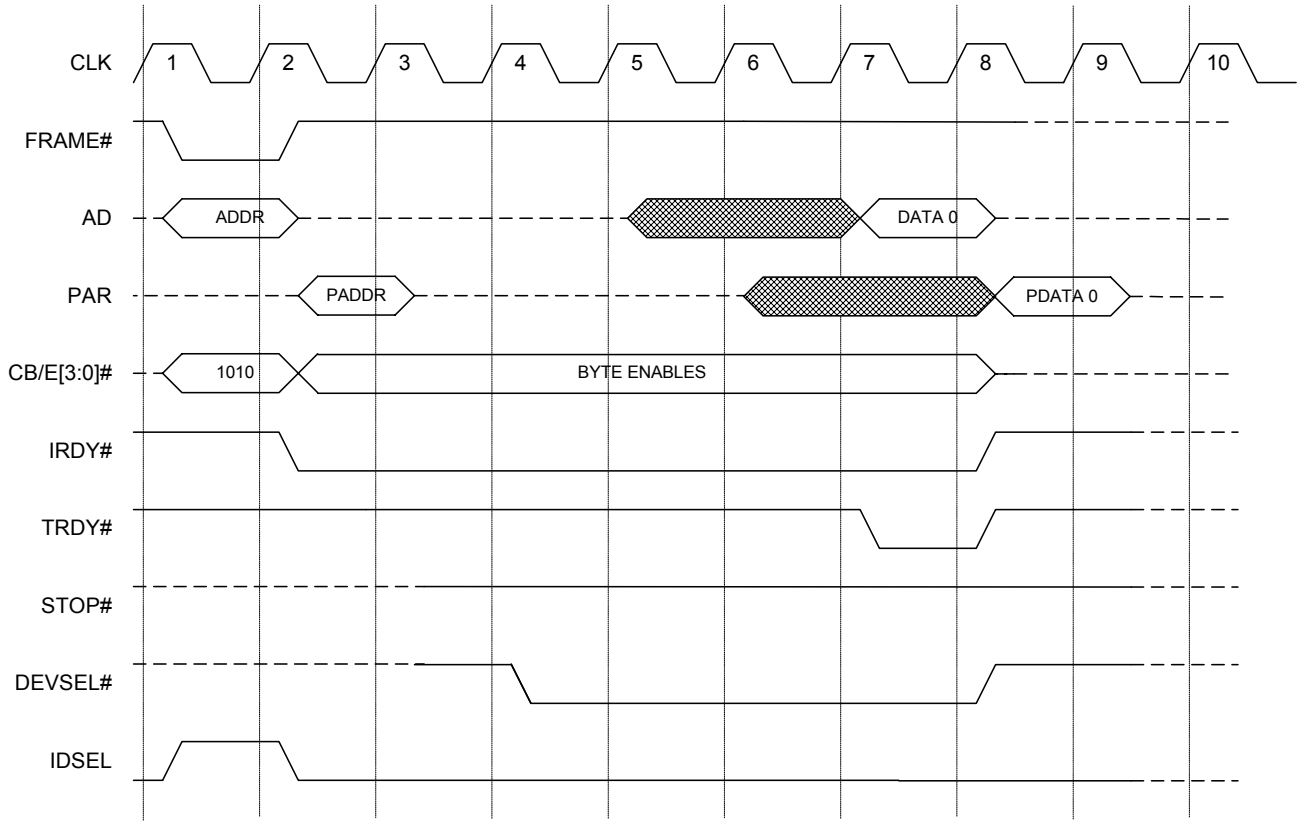
Each PCI device may implement a set of up to 256 internal registers that are used during system initialization to configure the device for proper operation in the system. To access the 1260-1XXX's configuration registers, a configuration read or write command must be initiated and the 1260-1XXX must sense its IDSEL input being asserted during the address phase of the bus cycle. The IDSEL acts as a chip select, AD[10:8] selects the function within the 1260-1XXX while the contents of AD[7:0] are used to select one of the 1260-1XXX's configuration registers within the given function. The 1260-1XXX is a single function device so there is only one set of configuration registers. **Figure 4-2** illustrates a configuration write cycle and **Figure 4-3** shows a configuration read cycle.



Notes:

1. If the 1260-1XXX's IDSEL is asserted when FRAME# is asserted and the commnad bus is '1011', then a configuration write cycle is indicated.
2. The 1260-1XXX claims the bus by asserting DEVSEL# in cycle 4.
3. Data is registered into the 1260-100X on the rising edge of cycle 5.
4. The single DWORD transfer completes when TRDY# is asserted in cycle 5 and de-asserted in cycle 6.

Figure 4-2 Configuration Write Cycle



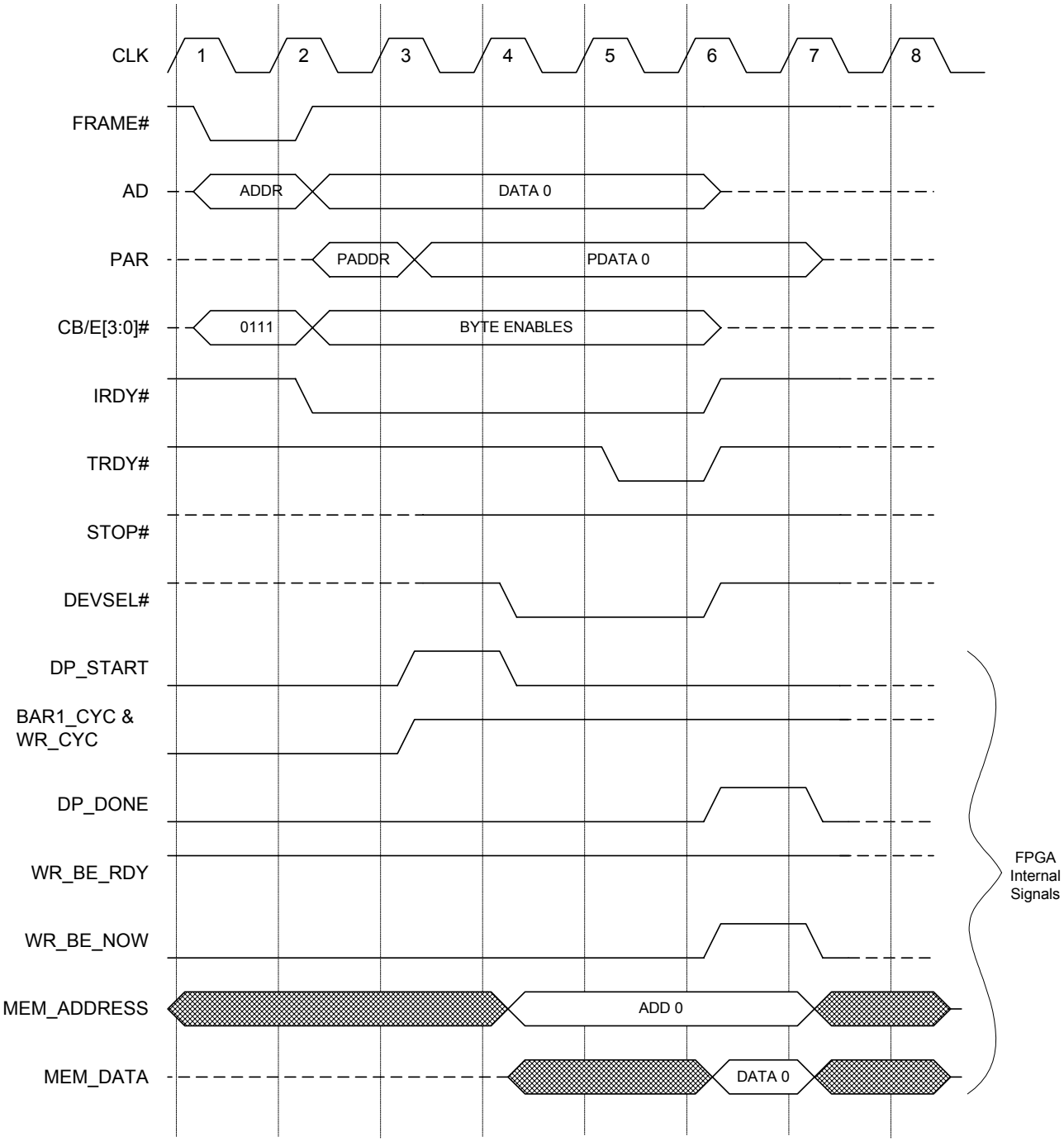
Notes:

1. If the 1260-1XXX's IDSEL is asserted when FRAME# is asserted and the commnad bus is '1010', then a configuration read cycle is indicated.
2. The 1260-1XXX claims the bus by asserting DEVSEL# in cycle 4.
3. During cycle 7, TRDY# is asserted and valid data is driven onto the PCI bus.
4. The single DWORD transfer completes when TRDY# is de-asserted in cycle 8.

Figure 4-3 Configuration Read Cycle

Memory Cycles

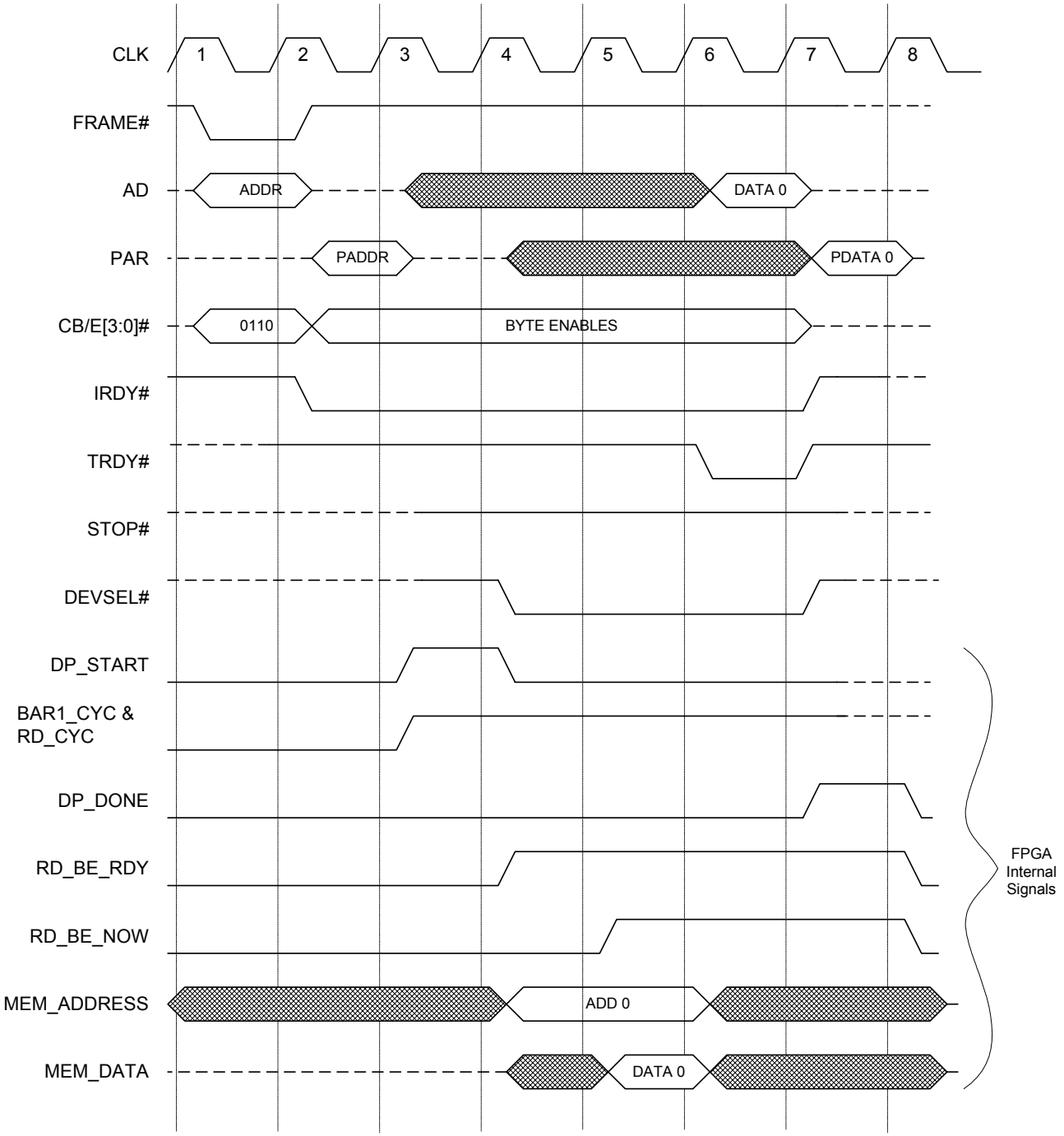
PCI memory cycles are used as memory mapped I/O to pass data to and from the Adapt-a-Switch Plug-in Module. During the address phase of a memory cycle, the AD bus has the address of the transfer while the C/BE[3:0]# has the command information. The address on the AD bus is compared with the value held in the Base Address Register to determine a hit for 1260-1XXX. During the data phase of the cycle a single byte of data is transferred on the 32-bit doubleword. This byte of data will reside in either byte 0 or byte 2 of the doubleword. **Figure 4-4** illustrates a memory write cycle and **Figure 4-5** shows a memory read cycle.



Notes:

1. When FRAME# is asserted and the commnad bus is '0111', then a write to memory space is indicated.
2. The 1260-1XXX will compare the address to the programmed space set in the memory base register.
3. If an address hit occurrs, the Target core asserts DP_START in cycle 3 and claims the PCI bus by asserting DEVSEL# in cycle 4.
4. Data transfer to the backend begins on the rising edge of cycle 7 and continues until the PCI bus ends the data transfer by de-assertion both FRAME# and IRDY#.
4. The single DWORD transfer completes when TRDY# is asserted in cycle 5 and de-asserted in cycle 6 and completes on the backend in cycle 7.

Figure 4-4 Memory Write Cycle



Notes:

1. When FRAME# is asserted and the commnad bus is '0110', then a read from memory space is indicated.
2. The 1260-1XXX will compare the address to the programmed space set in the memory base register.
3. If an address hit occurrs, the Target core asserts DP_START in cycle 3 and claims the PCI bus by asserting DEVSEL# in cycle 4.
4. Data transfer from the backend begins on the rising edge of cycle 7 and continues until the PCI bus ends the data transfer by de-assertion both FRAME# and IRDY#.
4. The single DWORD transfer completes when TRDY# is asserted in cycle 5 and de-asserted in cycle 6.

Figure 4-5 Memory Read Cycle

Adapt-a-Switch Bus

The Adapt-a-Switch Interface transfers data a byte at a time. The original interface did so in a serial bit-by-bit basis using an 8 MHz clock. The newer interface allows the data to transferred in parallel. The PXI to AaS Carrier supports both the serial and parallel bus of the Adapt-a-Switch Interface. The following sections describe the Adapt-a-Switch Bus.

Adapt-a-Switch® Plug-in Connector

The following signals are available on the Adapt-a-Switch® Module.

= Signals used only by original, serial interface.

= Signals used by original, serial and high-speed, parallel interfaces.

= Signals used only by high-speed, parallel interface.

= Signals NOT used.

Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	B1	HOLDOFF	C1	GND
A2	+24V	B2	LBOARDSELn	C2	HA01
A3	+24V	B3	HCLOCKIN	C3	HA02
A4	+12V	B4	HCLOCKOUT	C4	HA03
A5	+12V	B5	HDATAIN	C5	HA04
A6	+5V	B6	HDATAOUT	C6	HA05
A7	+5V	B7	HSTROBE	C7	HA06
A8	+5V	B8	HSHFTLD_HREAD	C8	HA07
A9	LIRQn	B9	ABUS0H	C9	HA08
A10	LRELAYRST	B10	ABUS0L	C10	HA09
A11	LLOGIC_RESET	B11	ABUS1H	C11	HDATA4

A12	HDATA0	B12	ABUS1L	C12	HDATA5
A13	HDATA1	B13	ABUS2H	C13	HDATA6
A14	HDATA2	B14	ABUS2L	C14	HDATA7
A15	HDATA3	B15	ABUS3H	C15	LFAST_CARD
A16	GND	B16	ABUS3L	C16	GND

Note- The following pins serve the same purpose for both parallel and serial plug-ins: +24V, +12V, +5V, GND, analog bus (ABUSxx), LIRQn, LRELAYRST, and LLOGIC_RST.

Adapt-a-Switch High-Speed Interface Signals

Signal Name	Type and Direction Relative to 1256	Description
LFAST_CARD	I (Open collector)	Tells the PXI to AaS Carrier which hardware handshake method the plug-in uses. • **Logic 1:** Indicates the original serial-data handshake. • **Logic 0:** Indicates the new, high-speed, parallel data handshake. This line has a 1K pull-up on the Carrier Adapt-a-Switch interface, so that the original handshake is the default mode. Plug-ins must not drive this line except when LBOARDSEL is active (low).
LBOARDSELn	O	Selects the plug-in for a bus cycle. This is used regardless of the handshake mode.
HDATA0 - HDATA7	I/O (Tri-state)	Data to and from the plug-ins. This is a tri-state, bi-directional bus. This bus is used only during high-speed handshake mode.
HSHFTLD_HREAD	O	This signal serves one of two purposes, depending on the mode: • **Original serial data mode:** This signal controls the mode (shift/load) of the output shift register. • **High-speed handshake mode:** This signal indicates the data direction (read or write). A logic 1 indicates a read cycle.
HHOLDOFF	I (Open collector)	When high, this signal stretches the bus cycle to accommodate slow devices. When the plug-in takes this signal low, the bus cycle will complete. For maximum speed, the plug-in should drive this signal low whenever LBOARDSEL is low. At all other times (when LBOARDSEL is not active), the plug-in should not drive HHOLDOFF. See HCLOCKIN for details about stretching the bus cycle.
HCLOCKIN	O	This signal works together with HHOLDOFF to determine the length of the bus cycle. This allows the high-speed interface to accommodate devices of various speeds.

Signal Name	Type and Direction Relative to 1256	Description
		For write operations: After LBOARDSEL goes low, the address and data from the PXI to AaS Carrier is already valid. The plug-in may use HCLOCKIN to clock the data from HDATA0-HDATA7 into a latch. The rising edge of HCLOCKIN occurs at least 60.6ns after LBOARDSEL and the address are valid. If the device requires additional time, then the plug-in should take HHOLDOFF high within 60ns after LBOARDSEL goes low. HCLOCKIN will then become a series of pulses. The first rising edge will occur at least 60.6ns after LBOARDSEL goes low, and will continue to clock at 60.6ns per cycle. HCLOCKIN will continue to clock until the plug-in takes HHOLDOFF low. Then HCLOCKIN will stop and the bus cycle will complete. Slow plug-ins may use HCLOCKIN as a timing source for controlling HHOLDOFF. For example, if a plug-in requires 150ns to stabilize its data on the bus, it can leave HHOLDOFF high until the third rising edge of HCLOCKIN occurs. The third rising edge allows 3 * 60.6ns = 181.8ns for the data to stabilize before the PXI to AaS Carrier latches it in. **For read operations:** After LBOARDSEL has gone low, the plug-in should place the addressed data on HDATA0-HDATA7. If the data will be stable within 60ns after LBOARDSEL goes low, then the plug-in should drive HHOLDOFF low within 60ns after LBOARDSEL goes low. This enables the fastest possible bus cycle. If the device being read requires more time, then the plug-in should take HHOLDOFF high within 60ns after LBOARDSEL goes low. HCLOCKIN will then become a series of pulses. The first rising edge will occur at least 60.6ns after LBOARDSEL goes low, and will continue to clock at 60.6ns per cycle. HCLOCKIN will continue to clock until the plug-in takes HHOLDOFF low. Then HCLOCKIN will stop and the bus cycle will complete. Slow plug-ins may use HCLOCKIN as a timing source for controlling HHOLDOFF.

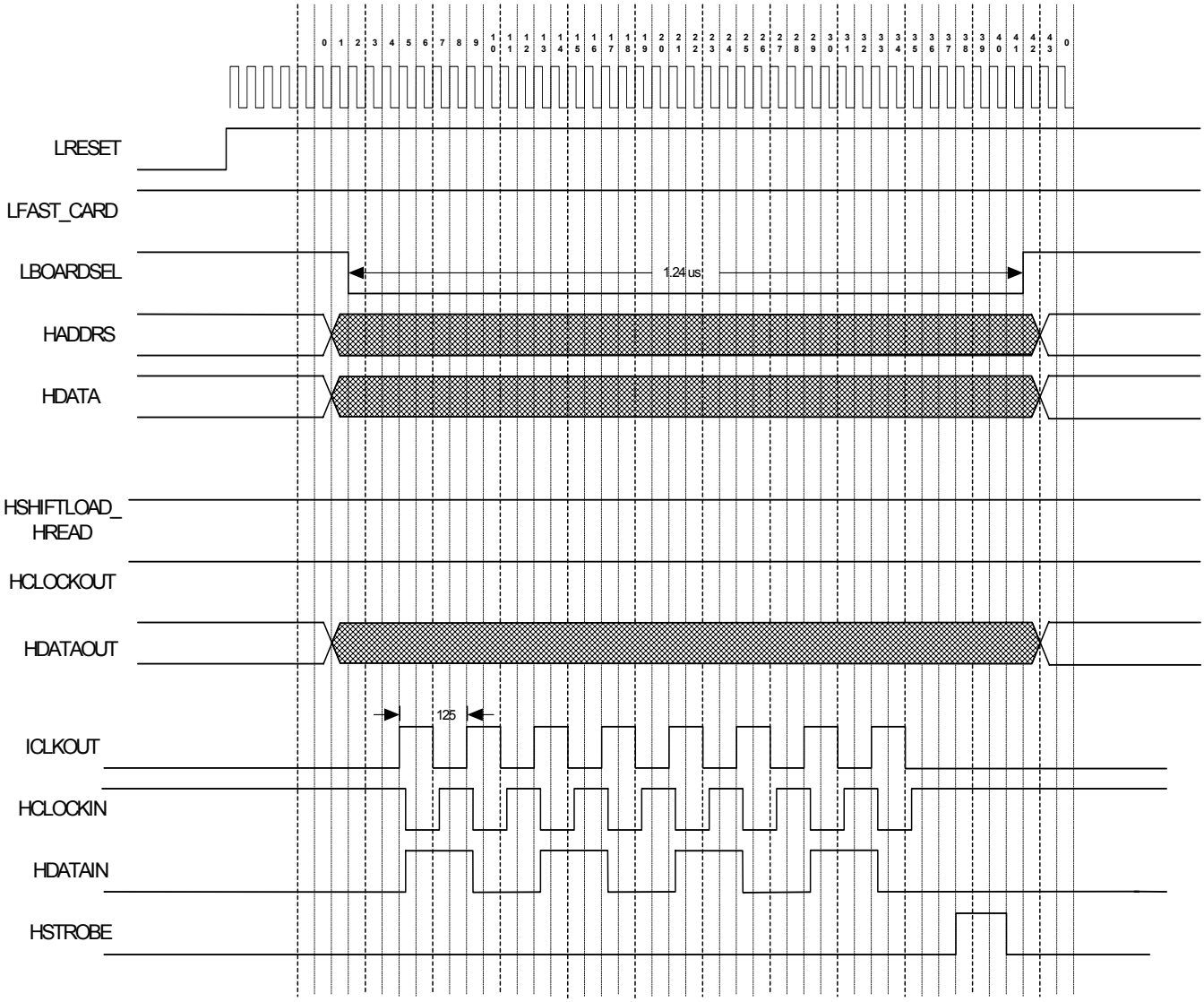


Figure 4-6 Adapt-a-Switch Serial Write Cycle

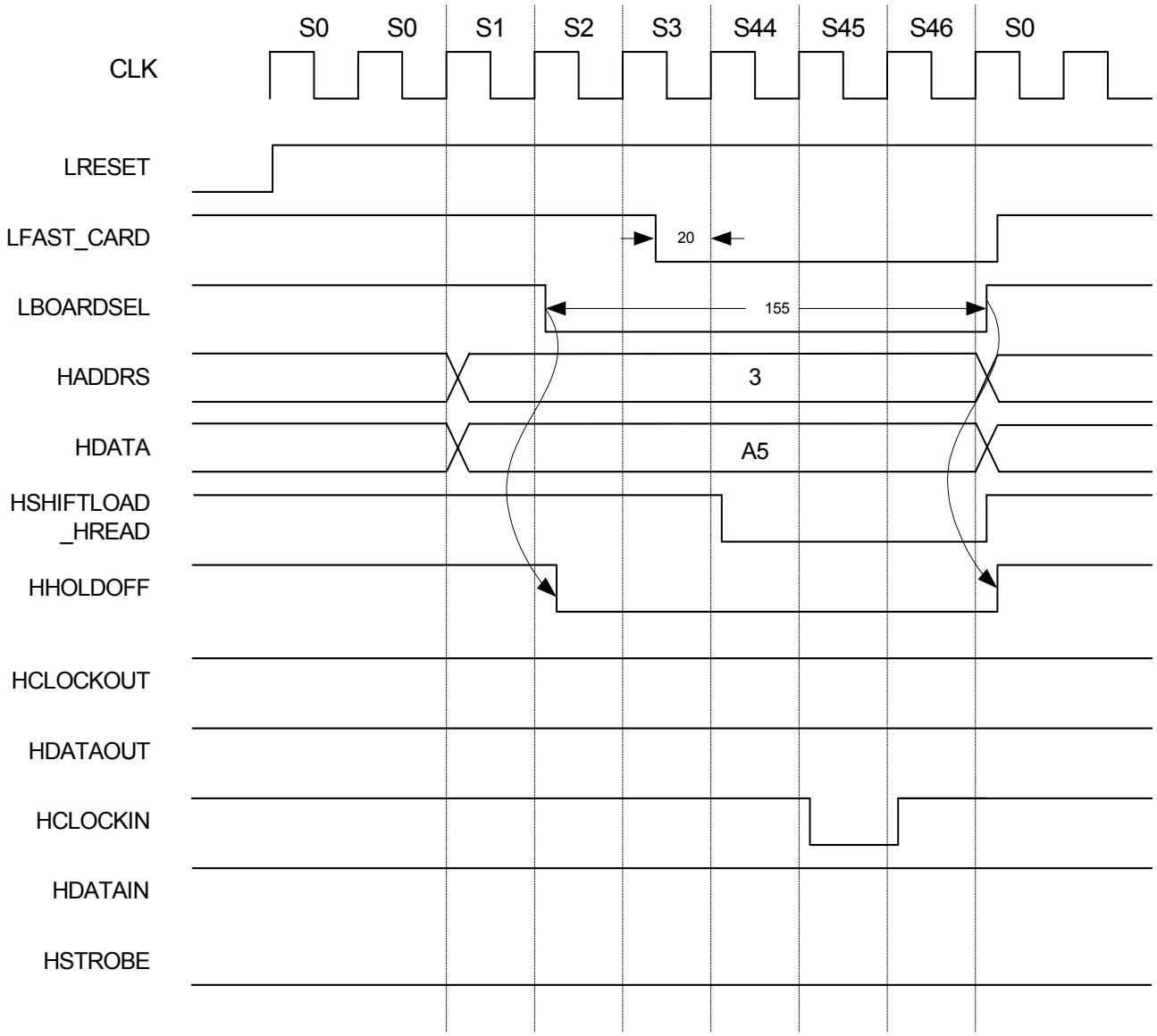


Figure 4-7 Adapt-a-Switch Parallel Write Cycle

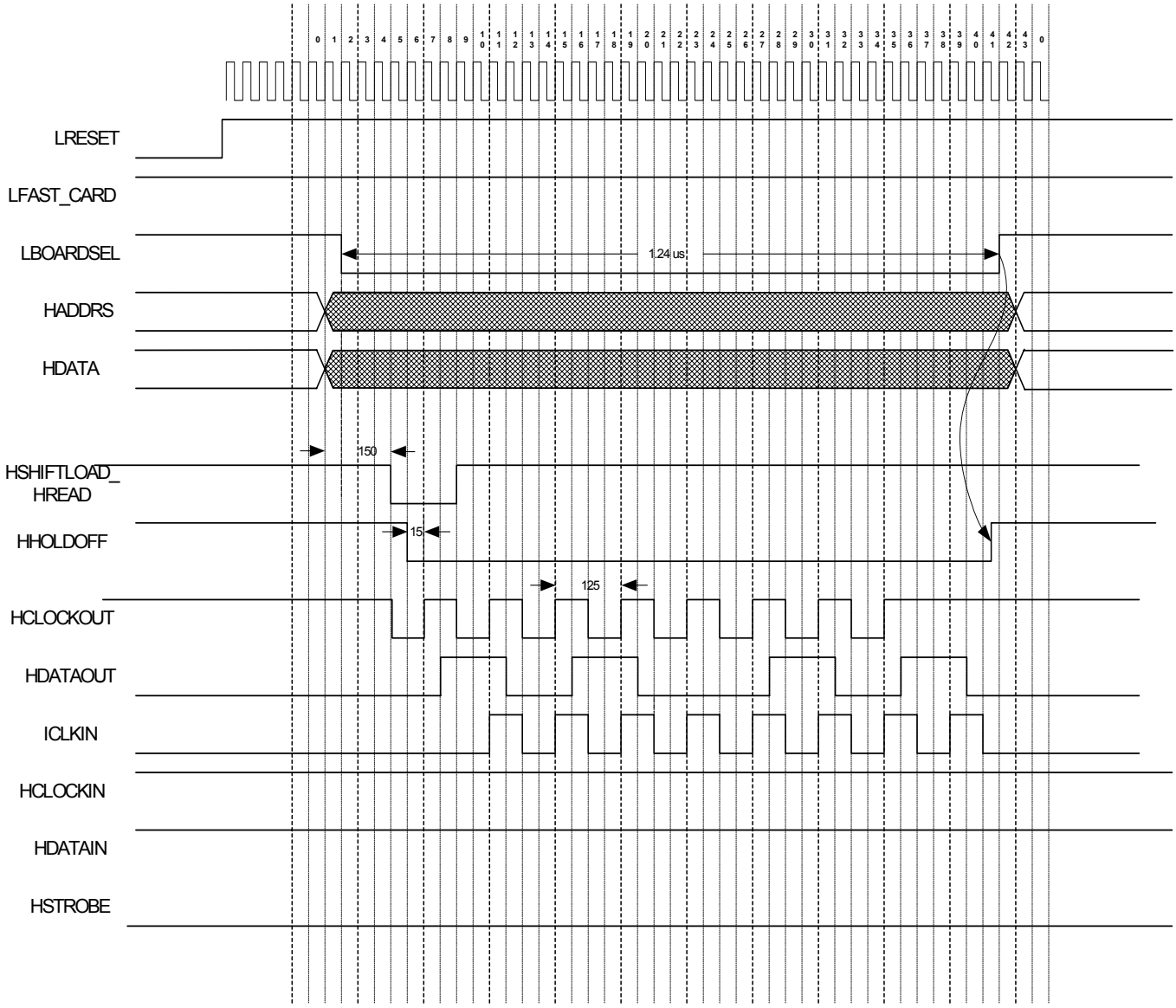


Figure 4-8 Adapt-a-Switch Serial Read Cycle

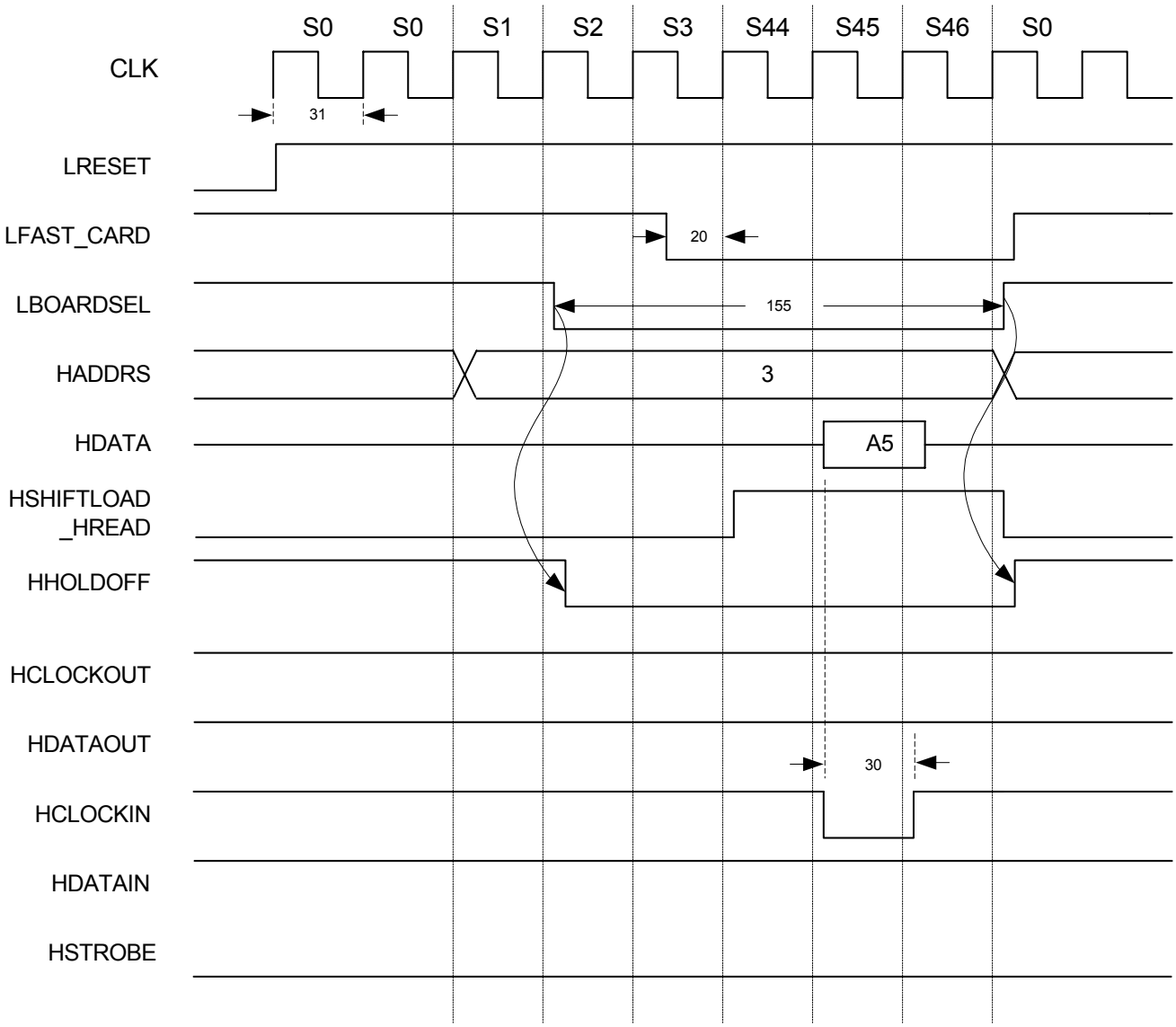


Figure 4-9 Adapt-a-Switch Parallel Read Cycle

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Chapter 5
PROGRAMMING

Software Drivers

The PXI to Adapt-a-Switch Plug-in Module comes with it's own software drivers (P/N 922050) for both LabView and CVI. A run-time library is also provided for the Soft Front Panel.

The following sections cover the functionality of registers that are accessed by the software driver. These registers are contained in the core of the FPGA.

Adapt-a-Switch Module Registers Base Address #0

Base Address Register #0 defines the memory address space that the Adapt-a-Switch Plug-in Module resides. It is through this address space that a PXI system is able to communicate with the registers on the Adapt-a-Switch Plug-in Module.

Table 5-1 shows an example of an Adapt-a-Switch Plug-in Module's registers and the associated address offset. For further information regarding the programming of an Adapt-a-Switch Plug-in Module, refer to the programming section in the appropriate Adapt-a-Switch manual.

Address Offset	Read	Write
0x000	Register #0	Register #0
0x002	Register #1	Register #1
0x200	ID Byte (resets descriptor address counter)	---
0x300	Timer Enable Status	---

Table 5-1 Adapt-a-Switch I/O Register Summary

Timer Registers Base Address #1

The general-purpose timer is contained in the PXI to AaS core. The Interrupt/Timer Registers consist of four memory-mapped I/O registers and are aligned on double-word boundaries. These registers reside in the memory address location defined by Base Address Register #1 in the Configuration Header. **Table 5-2** lists the Interrupt/Timer Registers and the associated address offset.

Address Offset	Read	Write
0x00	Interrupt Enable Status	Interrupt Enable Control
0x04	Timer Expired Status	Timer Expired Reset
0x08	---	Timer Count
0x0C	Timer Enable Status	Timer Enable Control

Table 5-2 Timer I/O Register Summary

Timer Register Definition

The first two registers are used in controlling the timer interrupt. In addition, the Interrupt Status Register has a bit dedicated for showing the state of the external (Adapt-a-Switch) interrupt line. The actual enabling and resetting of the external interrupt is left to the functionality of the particular Adapt-a-Switch Plug-in Module.

The second set of registers is used to control a general-purpose timer. A specific use for this timer is allowing software applications a method to provide relay-settling time. Default value for all registers is hex ‘00’ after reset. **Figure 5-1** shows an example of setting up a timer sequence.

Interrupt Enable Register (0x00, Rd/Wr)

Note - In order for a PXI interrupt to occur, the External Interrupt Enable bit in the Interrupt Control/Status register needs to be set to '1' and the Interrupt Disable bit of the Command register needs to set to '0' (both of these bits are located in the Configuration Header) in addition to either of the enable bits below.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Enable External Interrupt	Enable Timer Interrupt

Enable Timer Interrupt Bit

The timer interrupt is enabled when writing a '1' to this bit and disabled by writing a '0'. When this bit is set an interrupt will occur when the timer has expired. During a read, the state of the Enable Timer Interrupt bit can be sampled. This bit is set to '0' after reset.

Enable External Interrupt Bit

The external interrupt is enabled when writing a '1' to this bit and disabled by writing a '0'. When this bit is set an interrupt will occur when an external interrupt request from the Adapt-a-Switch module goes active. During a read, the state of the Enable External Interrupt bit can be sampled. This bit is set to '0' after reset.

Timer Expired Register (0x04, Rd/Wr)

Note- The Timer Expired bit resets the Timer Enable function located in the Timer Enable Register. Before trying to set the Timer Enable bit, to start a timing sequence, make the Timer Expired bit is reset. If not, the timing sequence will not start.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	External Interrupt	Timer Expired

Timer Expired Bit

This bit is set to '1' upon the completion of the timer's count. An interrupt will also be generated if the Enable Timer Interrupt bit was set. During a read, the state of the Timer Expired bit can be sampled. This bit will be set to '0' after a reset.

The Timer Expired bit can be reset when writing a '1' to this bit location. This bit must be reset before initiating another count sequence, since it disables the counter by resetting the Timer Enable bit in the Timer Enable Register.

External Interrupt Bit

During a read, the state of the External Interrupt signal coming from the Adapt-a-Switch module can be sampled. The External Interrupt bit is a read-only bit and cannot be reset from this register. The resetting of this bit must be preformed by a register function of the corresponding Adapt-a-Switch module.

Timer Count Register (0x08, Wr)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Timer Count 4	Timer Count 3	Timer Count 2	Timer Count 1	Timer Count 0

Timer Count

This register contains a 5 bit count value that is loaded into the timer. The count value of this register allows a timing interval between 1 to 16 ms in .5 ms increments. This register is a write-only register. This count value is set to '0' after reset. The following list the time duration for each of the count values:

Timer Count	Time Duration (ms)
00001	1.0
00010	1.5
00011	2.0
00100	2.5
00101	3.0
00110	3.5
00111	4.0
01000	4.5
01001	5.0
01010	5.5
01011	6.0
01100	6.5
01101	7.0
01110	7.5
01111	8.0
10000	8.5
10001	9.0
10010	9.5
10011	10.0
10100	10.5
10101	11.0
10110	11.5
10111	12.0
11000	12.5
11001	13.0
11010	13.5
11011	14.0
11100	14.5
11101	15.0
11110	15.5
11111	16.0

Timer Enable Register (0x0C, Rd/Wr)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Timer Enabled

Timer Enabled Bit

When this bit is set to '1', the timer begins counting. This bit is reset upon the completion of the timer's count. During a read, the state of the Timer Enabled bit can be sampled. This bit will be set to '0' after a reset.

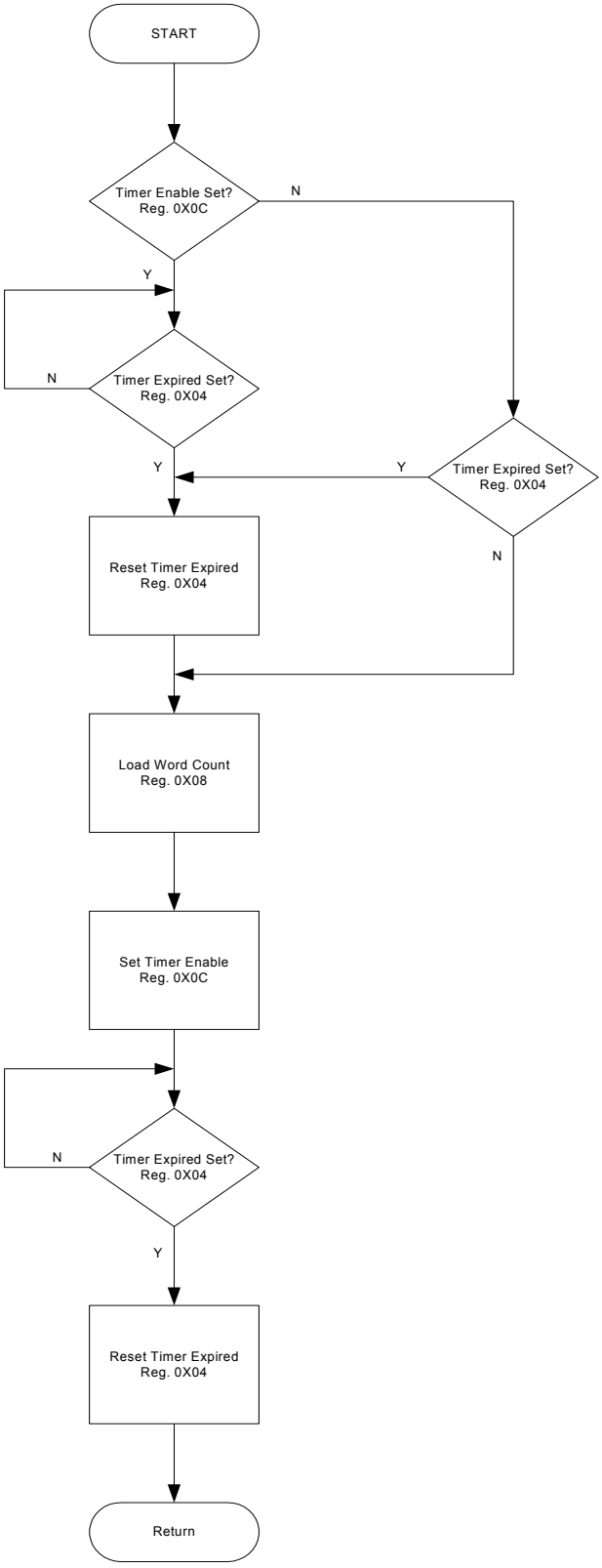

Figure 5-1 Setting Up a Timer Sequence

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Chapter 6
PRODUCT SUPPORT

Product Support

Racal Instruments has a complete Service and Parts Department. If you need technical assistance or should it be necessary to return your product for repair or calibration, call 1-800-722-3262. If parts are required to repair the product at your facility, call 1-949-859-8999 and ask for the Parts Department.

When sending your instrument in for repair, complete the form in the back of this manual.

For worldwide support and the office closes to your facility, refer to the Support Offices section on the following page.

Reshipment Instructions

Use the original packing material when returning the 1260-1XXX to Racal Instruments for calibration or servicing. The original shipping container and associated packaging material will provide the necessary protection for safe reshipment.

If the original packing material is unavailable, contact Racal Instruments Customer Service for information.

Support Offices

RACAL INSTRUMENTS

United States

(Corporate Headquarters and Service Center)
4 Goodyear Street, Irvine, CA 92618
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18 Avenue Dutartre, 78150 LeChesnay, France
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Racal Instruments Group Limited, Technologie Park,
D-51429 Bergisch Gladbach, Germany
Tel: +49 2204 844205; Fax: +49 2204 844219

Repair and Calibration Request Form

To allow us to better understand your repair requests, we suggest you use the following outline when calling and include a copy with your instrument to be sent to the Racal Instruments Repair Facility.

Model_____ Serial No._____ Date_____

Company Name_____ Purchase Order #_____

Billing Address_____

City

State/Province Zip/Postal Code Country

Shipping Address_____

City

State/Province Zip/Postal Code Country

Technical Contact_____ Phone Number ( )_____
Purchasing Contact_____ Phone Number ( )_____

1. Describe, in detail, the problem and symptoms you are having. Please include all set up details, such as input/output levels, frequencies, waveform details, etc.

2. If problem is occurring when unit is in remote, please list the program strings used and the controller type.

3. Please give any additional information you feel would be beneficial in facilitating a faster repair time (i.e., modifications, etc.)

4. Is calibration data required? Yes No (please circle one)

Call before shipping Ship instruments to nearest support office.
Note: We do not accept “collect” shipments.